REMARKS

Reconsideration and allowance are requested.

Claim 1 stands rejected under 35 U.S.C. §112, first and second paragraph. As discussed in a telephone interview with the Examiner on January 7, 2008, claim 1 is amended to return to the "operable" language to make clear that the decoder is operable in both, modes but of course not simultaneously. The Examiner agreed that this would overcome these rejections and that claim 1 would be interpreted in a similar fashion as method claim 12.

Claims 1-6, 8-17, 19-28, and 30-33 stand rejected as being anticipated by Qureshi et al. (2004/00308856). This rejection is respectfully traversed.

To establish that a claim is anticipated, the Examiner must point out where each and every limitation in the claim is found in a single prior art reference. *Scripps Clinic & Research Found. v. Genentec, Inc.*, 927 F.2d 1565 (Fed. Cir. 1991). Every limitation contained in the claims must be present in the reference, and if even one limitation is missing from the reference, then it does not anticipate the claim. *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565 (Fed. Cir. 1986). As will be explained below, Qureshi is missing at least one claim limitation in all the claims.

The technology in this case relates to a data processing system having multiple instruction sets and the way in which such multiple instruction sets may be encoded. A data processing system supporting multiple instruction sets allows considerable flexibility in the way in which program operations may be represented. For example, that flexibility can yield improved code density. But the typical trade-off is increased hardware to support the multiple instruction sets. The inventors overcame this problem by arranging the encoding of the instruction sets such that a common subset of instructions has the same encoding, (after

variations due to storage order, e.g. endianness, have been compensated for). As a result, the data processing system implementation can be advantageously simplified. As one example, common decoding logic may be more readily utilized, thereby reducing the hardware overhead needed.

The Examiner maps the claimed "an instruction decoder configured to decode program instructions specifying data processing operations to be performed by said data processing logic and to control said data processing logic to perform said data processing operations," as recited in claim 1, to address decode logic in Qureshi. But this address decoder is not an instruction decoder that decodes program instructions. Paragraph [0005] of Qureshi states: "An address is sent to the address decode logic corresponding to an endian accessible memory block. The decode logic uses the selected address and the endian selection register to remap the bytes of the selected address location so that the MSB [most significant byte] and LSB [least significant byte] are provided in the order expected by the operating system." Thus, this decode logic in Qureshi rearranges the order of the bytes of a selected address location. It does not decode program instructions. See also the discussion of address decode logic 511 in paragraph [0018].

Qureshi fails to disclose "said instruction decoder is operable in a first mode in which program instructions of a first instruction set are decoded and in a second mode in which program instructions of a second instruction set are decoded," as recited in claim 1. The Examiner contends that the claimed first mode is equivalent to the big endian mode of Qureshi, and the claimed second mode is equivalent to the little endian mode of Qureshi. But the big endian and little endian modes are simply different ways of storing data in a register. For example, in Tables 1 and 2 of Qureshi, the same piece of data ABCD059E is shown stored in big endian mode and in little endian mode. Qureshi does not identify this data as a program

instruction. However, even if the data of Qureshi was said to be a program instruction, it is clear that it would be the same instruction whether it is stored in big endian or little endian mode. Because the instructions stored in the big endian and little endian modes are the same instruction, an instruction stored in the big endian mode would be from the same instruction set as the instruction stored in the little endian mode. Thus, the two modes of Qureshi are not modes in which program instructions of a first instruction set and a second instruction set are decoded.

Qureshi also does not disclose "a subset of prograrn instructions of said first instruction set having a common bit-length and a common storage order compensated encoding with a subset of program instructions of said second instruction set such that, after compensating for storage order differences, all bits are identical." The Examiner appears to ignore the underlined language (added by amendment in the last response). In any event, because Qureshi only describes rearranging the order of storage for a single piece of data, it cannot disclose a subset of program instructions. Also, as shown above, a first instruction set and a second instruction set are not disclosed in Qureshi. So this claim feature cannot be disclosed by Qureshi.

Given that the claimed instruction decoder, first and second modes, and first and second instruction sets are not disclosed by Qureshi, Qureshi also lacks "forming a common subset of instructions representing at least one class of instructions, said common subset of instructions controlling said data processing logic to perform the same data processing operations independent of whether said instruction decoder is operating in said first mode or said second mode."

Thus, Qureshi lacks multiple features recited in the independent claims. McFarland overcome the deficiencies in Qureshi. Accordingly, the prior art rejections should be withdrawn.

The application is in condition for allowance. An early notice to that effect is respectfully requested.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 
John R. Lastova
Reg. No. 33,149

JRL:maa
901 North Glebe Road, 11th Floor
Arlington, VA 22203-1808
Telephone: (703) 816-4000
Facsimile: (703) 816-4100